

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Keith E. Kunz, et al. Docket No: TI-33676.1  
Serial No: Not Assigned Conf. No: Not Assigned  
Examiner: TBD Art Unit: TBD  
Filed: 07/14/2003  
For: DRAIN-EXTENDED MOS ESD PROTECTION STRUCTURE

**INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97 & 1.98**

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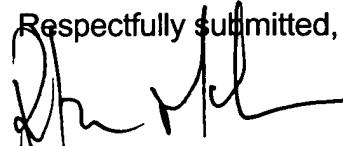
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Applicants wish to bring to the attention of the Patent and Trademark Office the information noted on the enclosed PTO/SB/08A. A copy of the noted references were provided in connection with the parent application and are therefore not being supplied herewith.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668, and please credit any excess fees to such Deposit Account. Any further necessary extension of time is hereby requested.

Respectfully submitted,

  
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Attorney for Applicants  
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Substitute for Form 1449A/PTO <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> (use as many sheets as necessary)				<b>Complete If Known</b>	
Sheet	1	of	1	Application Number	
				Filing Date	07/14/2003
				First Named Inventor	Keith E. Kunz, et al.
				Group Art Unit	
				Examiner Name	
				Attorney Docket No.	TI-33676.1

<b>U.S. PATENT DOCUMENTS</b>						
Exam. Initials*	Cite No. <sup>1</sup>	U.S. Patent Document		Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code <sup>2</sup> (if known)			
AA	4,692,781			Rountree et al.	09/08/1987	
AB	4,855,620			Duvvury et al.	08/08/1989	
AC	5,012,317			Rountree	04/30/1991	
AD	5,907,462			Chatterjee et al.	05/25/1999	
AE	5,940,258			Duvvury	08/17/1999	
AF						
AG						
AH						
AI						
AJ						

<b>FOREIGN PATENT DOCUMENTS</b>							
Exam. Initials*	Cite No. <sup>1</sup>	Foreign Patent Document		Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>3</sup>
		Office <sup>3</sup>	Number <sup>4</sup>				
BA							
BB							
BC							
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BG							
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<b>OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS</b>						
Exam. Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.				T <sup>2</sup>
CA		Rountree et al., "A Process-Tolerant Input Protection Circuit for Advanced CMOS Processes," 1988 EOS/ESD Symposium, pp. 201-05				
CB		Duvvury et al., "Substrate Pump NMOS for ESD Protection Applications," 2000 EOS/ESD Symposium, Paper 1A.2.1, pp. 7-17				
CC		Kunz et al., "5-V Tolerant Fail-safe ESD Solutions for 0.18 um Logic CMOS Process," 2001 ESD/EOS Symposium, September 11, 2001				
CD						
CE						
CF						
CG						
CH						
CI						
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup>Unique citation designation number. <sup>2</sup>Applicant is to place a check mark here if English Translation is attached.